49. (new) A method as in claim 48, wherein the dry etching comprises a first isotropic etching operation and a second anisotropic etching operation.

50. (new) A method as in claim 48, wherein the second insulating layer is isotropically etched.

51. (new) A method as in claim 48, wherein the first insulating layer is anisotropically etched.

52. (new) A method as in claim 48, wherein at least a side surface of the second protective insulating layer surrounding the electric connection region has a tapered surface with an acute angle to the top surface of the pad after the dry etching.

53. (new) A method as in claim 53, wherein an angle between the side surface of the second protective insulating layer surrounding the electric connection region and the top surface of the pad is smaller than a tapered angle between a side surface of the first protective insulating layer surrounding the electric connection region and the top surface of the pad.

54. (new) A method as in claim 48, wherein an angle between a side surface of the second protective insulating layer surrounding the electric connection region and a top surface of the pad is in the range of 30° to 60°.

55. (new) A method as in claim 54, wherein an angle between a side surface of a portion of the first protective insulation layer surrounding the electric connection region and the top surface of the pad is in the range of 60° to 90°.

56. (new) A method as in claim 48, wherein a distance between an upper end of a side surface of the first protective insulating layer surrounding the electric connection region and a lower end of the side surface of the second protective layer surrounding the electric connection region is in the range of 0 μm to 3 μm.

57. (new) A method as in claim 56, wherein the distance is in the range of 0 μm to 1 μm.

58. (new) A method as in claim 48, wherein an aperture formed in the second protective insulating layer after the dry etching is larger than an aperture formed in the first protective insulating layer after the dry etching.

59. (new) A method as in claim 48, comprising forming a bump electrode on the electric connection region in the pad through a barrier layer.

60. (new) A method as in claim 48, comprising forming the first insulating layer from a material comprising silicon oxide.

61. (new) A method as in claim 48, comprising forming the second insulating layer from a material comprising silicon nitride.

62. (new) A method as in claim 48, comprising forming the second protective insulating layer from a material comprising a nitride oxide layer.

63. (new) A method as in claim 48, comprising forming the pad on an insulation layer.

64. (new) A method for forming a bonding pad area using a dry etch process, comprising:

forming a conducting pad in electrical contact with an electronic device;

forming a protective insulation layer on a surface of the conducting pad, the protective insulation layer including at least first and second insulating layers, wherein the first insulating layer and the second insulating layer are formed from materials having different compositions, the first insulating layer being formed in direct contact with the surface of the conducting pad, the second insulating layer being formed in direct contact with the first insulating layer;

forming a mask in direct contact with a surface of the protective insulation layer and providing an opening in the mask; and

dry etching through the surface of the protective insulation layer at the opening in the mask to form an aperture extending through the second insulating layer and the first insulating layer to the surface of the pad, so that the second insulating layer includes a side surface surrounding the aperture, the second insulating layer side surface having a tapered shape with an angle in the range of 30 degrees to 60 degrees in relation to the surface of the conducting pad, and the first insulating layer includes a side surface surrounding the aperture, the first insulating layer side surface having a tapered shape with an angle in the range of 60 degrees to 90 degrees in relation to the surface of the conducting pad.

65. (new) A method as in claim 64, wherein the protective insulation layer consists of the first insulating layer and the second insulating layer.

66. (new) A method as in claim 65, wherein the first insulating layer comprises an oxide and the second insulating layer comprises a nitride.

67. (new) A method as in claim 64, wherein the dry etching includes an isotropic etching operation followed by an anisotropic etching operation.

68. (new) A method of fabricating a semiconductor device comprising:

forming a pad with a predetermined pattern on an insulating layer;

forming a protective insulating layer on a surface of the pad;

forming a mask layer in direct contact with a surface of the protective insulating layer, the mask layer having an aperture in a region corresponding to an electrical connection region of the pad; and

dry etching through the surface of the protective insulating layer to form an opening extending through the protective insulating layer to the electrical connection region of the pad, so that the protective insulating layer includes a side surface surrounding the opening, the side surface being tapered so that a diameter of the protective insulation layer at the pad surface is smaller than a diameter of the protective insulation layer a distance away from the pad surface.

69. (new) A method as in claim 68, wherein wherein the protective insulating layer has a thickness of 1000 nm to 2000 nm.

70. (new) The method of fabricating a semiconductor device of claim 68, wherein a tapered angle between the side surface of the insulating layer surrounding the electric connection region and the top surface of the pad is in the range of 10° to 80°.

71. (new) The method of fabricating a semiconductor device of claim 68, wherein a bump electrode is provided on the electric connection region of the pad through a barrier layer.

72. (new) The method of fabricating a semiconductor device of claim 68, wherein the protective insulating layer is formed from a material including one of a silicon oxide layer and a silicon nitride layer.--